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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Michael A. Bernadicou
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

EXAMINER	
SMITH, FRANCIS P	
ART UNIT	PAPER NUMBER
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,716	DAVIS ET AL.	
	Examiner	Art Unit	
	Francis P. Smith	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,14-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,14-21,23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments as per the amended claims filed February 19, 2009 have been fully considered but they are not persuasive as outlined herein. Applicants have amended the claims to overcome the rejection of the previous office action, as discussed during the interview on January 28, 2009. However, upon additional search and consideration as per the claim amendment, a new rejection is presented herein. Claims 1, 4 and 15 are currently amended. Claims 3 and 22 are canceled. Claims 1, 2, 4-21, and 23 are currently pending and examined on the merits.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2, 9-14, 16-19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca et al. (US 2002/0094686 A1) in view of Boggs (US 6,087,191).

Gorczyca teaches treating the surface of a semiconductor article such that the surface is treated to render said surface less prone to cracking and to extend the useful life of the article comprising:

roughening a surface of the substrate, wherein the roughening produces microfissures therein ([0017], [0018], and lines 2-4 of [0022]);

treating the roughened surface with a strong acid ([0022], [0028]); and

applying a silicon coating which is then converted to silicon oxide onto the roughened surface, wherein applying a coating composition onto the roughened surface includes filling and covering the microfissures (e.g. a dielectric coating composition containing at least one metal oxide) ([0023], [0034]). Furthermore, it would have been obvious to one having ordinary skill in the art at the time of the invention to apply the

silicon oxide layer directly, thereby saving time and processing costs associated with the extra conversion step from silicon to silicon oxide. Gorczyca does not expressly teach that the dielectric coating composition is selected from one of aluminum, zirconium, or yttrium oxides.

Boggs teaches the repair of surface defects on semiconductor wafers that form during semiconductor processing. Boggs discloses that silicon oxide and zirconium oxide were known equivalent fill materials at the time of the invention (col. 2, lines 45-61). Therefore, it would have been well within the level of ordinary skill in the art at the time of the invention to apply zirconium oxide in Gorczyca in lieu of silicon oxide since Boggs teaches their equivalence.

Regarding claim 2, Gorczyca teaches a quartz substrate [0014].

As for claims 9 and 10, the quartz article is roughened by sand blasting using abrasive material with size ranges between 1-800 microns, and thus, would inherently produce a surface roughness within the claimed range of 180-320 and 200-300 micro inch Ra [0018].

Claims 11-14, the roughened surface is treated with a strong acid comprising immersing the substrate in an immersion bath comprising a strong acid (hydrofluoric acid) at a concentration of >0-70 volume percent (i.e. within the claimed range of 15-50 and 25-35 volume percent) [0028].

Addressing claims 16 and 17, micro cracks caused by mechanically roughening which appear as breaks in the quartz glassy structure propagating from the treated surface into the quartz for distances up to 200 micrometers (i.e. the depth of the

microfissures is up to about 0.005 inch and 0.006 inch) [0022].

Regarding claim 23, the surface of a quartz substrate is roughened (i.e. microparticles of the substrate material are inherently left on the roughened surface), said roughened surface is subsequently treated with a strong acid whereby at least some of the microparticles of the substrate material are removed from the roughened surface.

For claims 18 and 19, Gorczyca teaches forming micro cracks in the surface of quartz substrates at a depth of about 0.0078 inch, which is subsequently filled using silicon dioxide ([0022], [0023], [0034]). Therefore, the applied coating will inherently have a thickness with in the claimed range of up to 0.010 and 0.003 inch.

6. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca et al. (US 2002/0094686 A1) and Boggs (US 6,087,191) as applied to claim 1, in view of Choi (US 6,833,279 B2).

Regarding claims 4 and 15, Gorczyca/Boggs teach applying a metal oxide coating composition onto the roughened surface comprising zirconium and aluminum oxides (see Boggs: col. 2, lines 45-61), but does not expressly teach applying a coating to the roughened surface with a composition comprising zirconium oxide and yttrium oxide.

Choi teaches a method of fabricating and repairing ceramic components for use in semiconductor fabrication. Specifically, Choi teaches an alumina or a yttrium oxide layer (i.e. a dielectric coating) deposited on a roughened ceramic surface. The layer is

deposited via a plasma spray process, which is necessarily provided by a plasma generating gas whereby the plasma spray is directed toward the roughened surface in order to apply said layer to said roughened surface (col. 3, line 38-col. 4, line 26). Gorczyca and Choi are analogous art because they are from the same field of endeavor: preparing/repairing components for subsequent semiconductor processing steps. Therefore, one having ordinary skill in the art at the time of the invention would have looked to Choi to deposit a yttrium oxide layer on the semiconductor surface in lieu of aluminum oxide (e.g. alumina) in Gorczyca/Bogg's method since Choi teaches the equivalence of alumina and yttrium oxide.

7. Claims 5-8, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorczyca et al. (US 2002/0094686 A1) and Boggs (US 6,087,191) as applied to claim 1, and further in view of Kowalsky et al. (US 6,861,101 B1) and Choi (US 6,833,279 B2).

Gorczyca/Boggs discloses applying a coating composition to a roughened surface, but does not expressly teach applying a coating composition by generating a plasma spray.

Kowalsky teaches a method whereby particles of metals, ceramics, or mixtures thereof may be applied to a substrate using a plasma spray coating method. As per claims 5 and 20, Kowalsky teaches applying a coating composition onto a surface by providing a plasma generating gas (e.g. argon, nitrogen, hydrogen, and compressed air as per claims 6 and 8) and the coating composition to a plasma torch/gun at a high

temperature of 8,000-12,000°F (within the claimed temperature range of claims 7 and 21), whereby the resulting plasma spray is directed to the substrate (col. 2, line 66-col. 3, line15; col. 6, line 45-col. 7, line 16). The advantage of utilizing Kowalsky's plasma spray method is that materials of a wide range of particle sizes may be deposited with high velocity (col. 4, lines 28-31). Choi teaches that it was known in the art at the time of the invention to utilize a plasma spray process to deposit a coating composition layer on a roughened component for semiconductor processing (col. 3, lines 38-50; col. 4, lines 1-6). Therefore, one having ordinary skill in the art at the time of the invention, motivated by Choi, would have utilized Kowalsky's plasma spray process in Gorczyca's method in order to apply coating materials of a wide range of particle sizes on a roughened surface at velocity sufficient to form a layer of said materials.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Francis P. Smith whose telephone number is (571) 270-3717. The examiner can normally be reached on Monday through Thursday 7:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mikhail Kornakov can be reached on (571) 272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/F. P. S./

Examiner, Art Unit 1792
/Michael Kornakov/
Supervisory Patent Examiner, Art Unit 1792